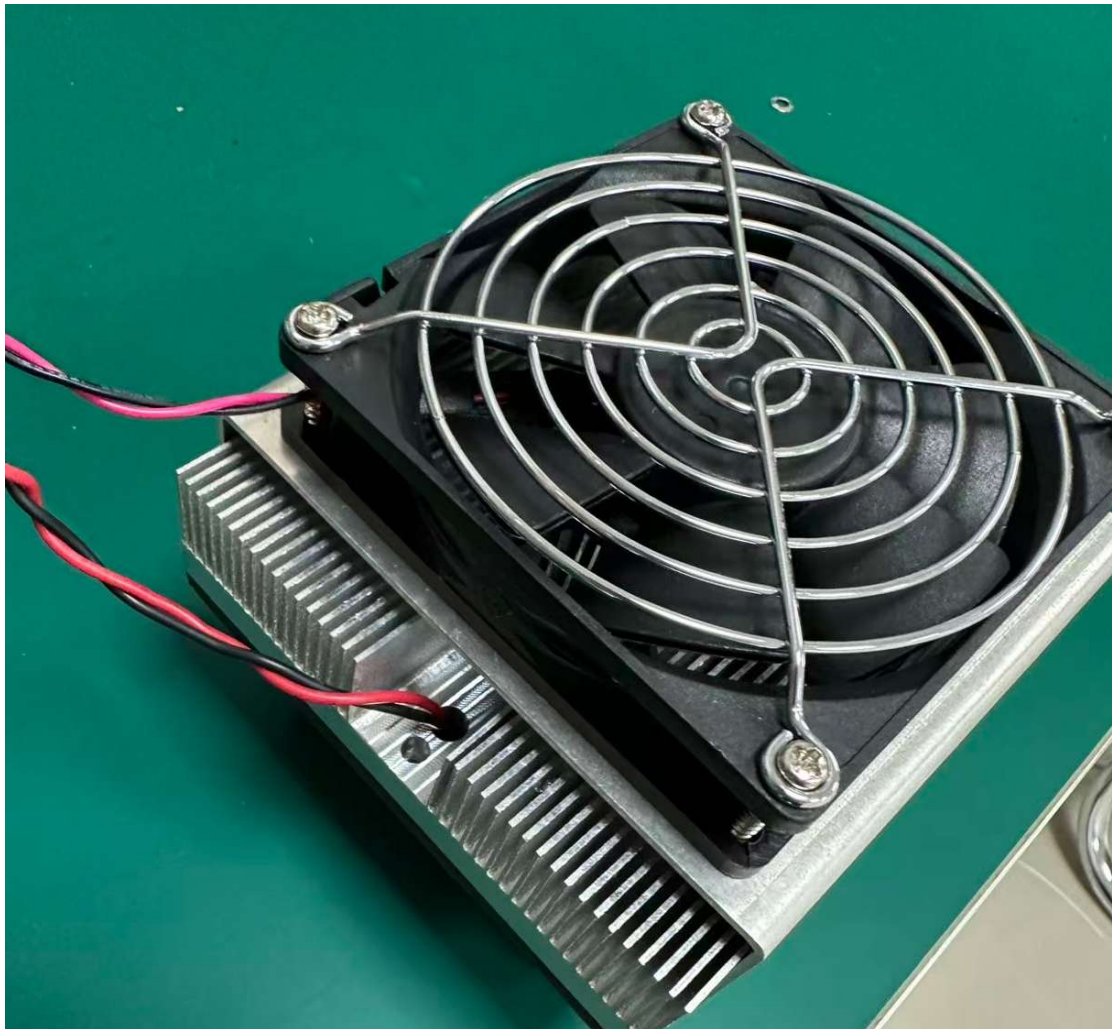


Heat Dissipation Challenges of High-Density Thermoelectric Cooler Arrays: Optimization Design of Multi-Chip Stack Heat Dissipation



1. Abstract

High-density Thermoelectric Cooler array combined refrigeration serves as the core implementation solution for industrial precision temperature control, large-scale cold

chain equipment, and multi-zone constant temperature systems. Compared with single-chip refrigeration, the multi-chip stacked array structure delivers ultra-high cooling power and wide-range temperature control coverage, yet it also brings common industrial challenges including concentrated heat accumulation, uneven chip temperature distribution and single-device performance attenuation. Focusing on the core heat dissipation pain points of Thermoelectric Cooler arrays, this paper deeply analyzes the heat accumulation mechanism of densely arranged multi-chip structures. Combined with ZICOTEC's field-tested industrial thermal management experience, it systematically proposes comprehensive multi-chip stack heat dissipation optimization solutions covering chip spacing design, air duct layout optimization, integrated water cooling plate adaptation and transformation, and thermal simulation verification. With dual validation of simulation analysis and actual test data, this article compares temperature rise differences, temperature uniformity and refrigeration stability before and after optimization. Finally, standardized industrial design specifications for array refrigeration are summarized, effectively solving overheating, power imbalance and inconsistent service life of high-density TEC arrays during long-term operation. It provides authoritative practical guidance for structural design and heat dissipation iteration of high-power array semiconductor refrigeration equipment.

Keywords: Thermoelectric Cooler array cooling, chip stacking heat dissipation optimization

Meta Description: Solve Thermoelectric Cooler array heat accumulation with ZICOTEC optimized stacking and cooling design.

2. Heat Accumulation Principle of Array Arrangement

High-density Thermoelectric Cooler arrays achieve multiple improvements in cooling power through dense stacking and parallel cooperative operation of multiple TEC chips, which are widely applied in high-power scenarios such as industrial precision constant temperature, medical precision temperature control and commercial cold chain systems. However, the densely arranged structural characteristics fundamentally cause heat accumulation and heat dissipation failure, becoming the key technical difficulty different from single-chip heat dissipation. A single TEC chip only needs to export heat from a single hot spot, while densely arranged multi-chip arrays form regional concentrated heat sources with mutual heat superposition and convection interference, breaking the heat balance logic of conventional single-chip heat dissipation.

From the perspective of thermodynamics, heat generated by the hot end of a single working TEC chip diffuses freely to the surrounding space with smooth heat dissipation paths and uniform thermal field distribution. In high-density array layouts, adjacent Thermoelectric Cooler chips are arranged with extremely narrow spacing. Waste heat released by each hot end forms cross thermal interference, and mutual radiation and convection superposition create a closed high-temperature zone in the central area of the array. Chips located in the center face far worse heat dissipation conditions than edge chips, resulting in an extreme temperature imbalance

phenomenon of **central heat accumulation and low edge temperature**, which is the primary cause of failures in array refrigeration equipment.

According to massive field test data from ZICOTEC, unoptimized dense TEC arrays present a steady-state temperature rise of central chips 15~25°C higher than edge chips, keeping central chips working under long-term high-temperature overload conditions. Severe temperature imbalance leads to inconsistent cooling power of each chip in the array, causing partial full-load operation and partial idle performance, which greatly reduces overall refrigeration efficiency. Meanwhile, continuous high-temperature heat accumulation accelerates the aging of internal thermoelectric grains, resulting in inconsistent chip service life and higher equipment failure and operation maintenance costs. In addition, hot air backflow and air duct turbulence during multi-chip stacked operation further aggravate heat accumulation and form a vicious cycle.

3. Optimization Scheme of Chip Spacing Design and Air Duct Layout

For heat accumulation and temperature unevenness caused by dense arrangement of Thermoelectric Cooler arrays, standardized chip spacing design and air duct structure optimization are the lowest-cost, most implementable and widely adaptable basic optimization methods. These solutions greatly improve the disordered thermal field of arrays without modifying core heat dissipation hardware, and are compatible with conventional heat dissipation systems such as air cooling and heat pipe cooling.

In terms of chip spacing design, the industry generally has a misunderstanding that dense arrangement brings higher power density. Excessively reduced chip spacing is the main artificial factor causing heat accumulation. Based on multiple sets of array condition tests, ZICOTEC summarizes industrial standardized spacing specifications: the center spacing of conventional high-power TEC array chips should be controlled within **35~45mm**, with a minimum spacing of no less than 30mm. This standard spacing ensures overall equipment power density while completely avoiding cross thermal radiation interference between adjacent chips and reserving sufficient space for heat diffusion and air circulation. For ultra-compact high-density equipment that cannot meet standard spacing requirements, a density zoning layout is adopted to divide the array into independent heat dissipation units with dedicated isolation air ducts between units to block cross heat superposition.

In terms of air duct layout optimization, traditional closed straight air ducts easily generate turbulence and thermal backflow, preventing rapid heat discharge from the array center. To solve this problem, ZICOTEC adopts a customized directional flow guiding air duct scheme. Abandoning the traditional flat air duct structure, it applies a **single-side air intake, double-side air outlet and zonal flow guiding** design, matching independent air duct channels for each TEC unit to avoid mixing of cold and hot air and heat backflow. Meanwhile, the angles of wind deflectors and flow guides are optimized to guide low-temperature ambient air to preferentially flush the high-temperature central area of the array, specifically solving central heat

accumulation problems.

For air-cooled array equipment, ZICOTEC further optimizes fan layout logic. Instead of global unified air supply, zonal independent temperature-controlled air supply is adopted to match corresponding air volume according to temperature rise differences in different array areas. Conventional air supply is applied to low-temperature edge areas while enhanced air supply is implemented for high-temperature central areas, accurately balancing the overall temperature uniformity of the array. This solution effectively reduces the overall temperature rise of the array without increasing power consumption and noise, solving the problem of uneven heat dissipation in multi-chip stacking systems.

4. Adaptive Modification of Integrated Water Cooling Plate for Array Chips

For ultra-high-power, 24-hour continuous operating and high-density Thermoelectric Cooler array working conditions, conventional air cooling and air duct optimization have limited heat dissipation ceilings and cannot completely eliminate concentrated heat accumulation. ZICOTEC's customized integrated micro-channel water cooling plate exclusive for multi-chip stacked arrays is currently the optimal industrial-grade heat dissipation solution for high-density TEC arrays, thoroughly solving core pain points such as array temperature unevenness, high-temperature performance attenuation and thermal fatigue damage.

Different from traditional independent single-chip water cooling plates, the ZICOTEC integrated array water cooling plate adopts an integral forming structure without splicing gaps or segmented thermal resistance, covering the entire TEC array to realize full-domain uniform heat exchange. Targeting severe central heat accumulation, the water cooling plate adopts a **zoned differentiated micro-channel design**. The high-temperature central area is equipped with denser flow channels and smaller channel spacing to increase exchange flow and heat dissipation efficiency, while conventional flow channels are arranged in low-temperature edge areas to balance overall heat dissipation performance, fundamentally eliminating array temperature imbalance through hardware structural optimization.

In terms of structural adaptation and modification, the surface of the integrated water cooling plate adopts high-precision polishing technology with a flatness error controlled within 0.05mm, ensuring uniform fitting of every Thermoelectric Cooler chip in the array. Combined with the standardized 0.08~0.12mm thermal grease coating process, local excessive contact thermal resistance is completely eliminated, realizing synchronous, rapid and uniform heat export from all chip hot ends. Meanwhile, the water cooling plate adopts a diagonal inlet and outlet flow guiding design to avoid medium short-circuit flow and ensure the coolant fully flows through all heat exchange areas without dead zones.

Compared with segmented water cooling solutions, the ZICOTEC integrated array water cooling plate greatly simplifies the pipeline structure of equipment, reduces liquid leakage risks and assembly errors, and avoids inconsistent heat exchange and

uneven pipeline pressure drop caused by split water cooling structures. It is suitable for mass production and assembly of large-scale TEC arrays, controlling the temperature difference of all chips within $\pm 1^{\circ}\text{C}$, far exceeding the temperature control accuracy of conventional heat dissipation schemes, and significantly improving the refrigeration stability and service life of array equipment.

5. Thermal Simulation Verification of Heat Dissipation Performance

To quantitatively verify the optimization effects of spacing adjustment, air duct transformation and integrated water cooling plates, ZICOTEC builds high-density Thermoelectric Cooler array models with consistent power and layout density through professional thermal simulation software. Steady-state thermal simulation comparison tests are conducted on the original unoptimized structure, air duct optimized structure and integrated water cooling optimized structure under industrial full-load continuous operating conditions. Four core indicators including maximum temperature, minimum temperature, overall temperature difference and steady-state temperature rise of the array are collected for comparative analysis.

Original unoptimized array model: With dense arrangement, conventional straight air ducts and split heat dissipation structure, the maximum temperature of central chips reaches 78.6°C and the minimum edge temperature is 49.2°C after full-load steady-state operation. The maximum overall array temperature difference reaches 29.4°C , with severe central heat accumulation and obvious chip temperature imbalance and refrigeration power attenuation, posing overheating and burnout risks during long-term operation.

Spacing and air duct optimized model: After standardized spacing adjustment and zonal flow guiding air duct transformation, the overall heat dissipation environment of the array is significantly improved. The maximum steady-state temperature under full load drops to 62.3°C and the minimum temperature is 48.5°C , with the overall temperature difference reduced to 13.8°C . Heat accumulation is effectively relieved and chip temperature uniformity is greatly improved, though slight overheating still exists in the central area under ultra-high-density extreme working conditions.

Integrated water cooling plate optimized model: Equipped with ZICOTEC exclusive micro-channel water cooling structure for arrays, the heat dissipation performance achieves qualitative improvement. The maximum steady-state temperature under continuous full-load operation is only 45.1°C and the minimum temperature is 43.8°C , with the maximum temperature difference of the entire array controlled within 1.3°C . No local heat accumulation or temperature imbalance occurs, and the thermal field presents highly uniform distribution. All chips operate in a low-temperature and low-load state, completely solving the heat dissipation difficulties of high-density multi-chip stacking systems.

Simulation results fully prove that basic spacing and air duct optimization solves conventional heat dissipation problems of medium and low-density arrays and serves as the preferred low-cost optimization scheme. In contrast, the integrated micro-

channel water cooling structure is the ultimate heat dissipation solution for high-density, high-power and long-term operating Thermoelectric Cooler arrays, fully meeting industrial high-precision and high-stability temperature control requirements.

6. Conclusion: Industrial Design Specifications for Array Refrigeration

Combined with heat accumulation mechanism analysis, structural optimization schemes and simulation verification data, and based on ZICOTEC's rich engineering experience in industrial TEC array refrigeration projects, this paper summarizes a set of implementable standardized industrial design specifications for high-density Thermoelectric Cooler multi-chip stacked equipment. Covering the whole process of structural arrangement, air duct design, heat dissipation selection and hardware adaptation, the specifications eliminate array heat accumulation, temperature unevenness and performance attenuation from the source.

First, standardize array arrangement. Strictly control chip layout spacing. The center spacing of conventional industrial arrays shall not be less than 35mm. Ultra-high-density equipment adopts zonal unit layout with independent heat dissipation air ducts reserved to avoid cross thermal interference between adjacent chips and reduce the root cause of heat accumulation.

Second, refine air duct layout. Abandon traditional straight turbulent air ducts and adopt zonal flow guiding and directional air supply structures. Strengthen air circulation in high-temperature central areas and optimize fan control logic to implement differentiated heat dissipation and balance the global thermal field.

Third, classify and select heat dissipation schemes. For medium and low-density arrays working intermittently, prioritize air cooling schemes optimized by spacing and air duct adjustment for higher cost performance. For high-density, high-power and 24-hour continuous operating industrial precision arrays, ZICOTEC integrated micro-channel water cooling plates are mandatory to ensure full-domain heat dissipation uniformity and long-term operational stability.

Fourth, standardize assembly processes. Ensure flat and uniform contact surfaces during array chip assembly, and strictly implement standardized thermal medium coating processes to eliminate local thermal resistance differences and avoid secondary temperature imbalance caused by assembly defects.

In general, the core optimization focus of high-density Thermoelectric Cooler array refrigeration is not simply increasing cooling power, but solving uneven heat dissipation and concentrated heat accumulation. Following standardized industrial design specifications and adopting ZICOTEC exclusive array heat dissipation optimization solutions can maximize the performance of multi-chip stacked refrigeration systems, thoroughly solve industrial pain points such as temperature control drift, performance attenuation and premature chip aging of array equipment, and guarantee long-term stable operation of high-power semiconductor refrigeration equipment.